Sensitivity of FinFET Performance to Lateral Gate Misalignment
CM2-13

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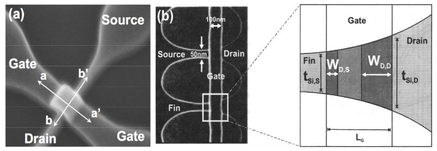
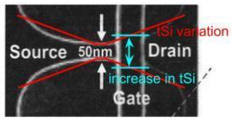
Overview

A major crisis faced by the technology industry today is the end of the exponential growth of its key driving force, the number of transistors on a chip. Traditionally, this trend is achieved by making the transistors smaller, a challenging task in the nano-scale regime. To solve this problem, new transistor structures are proposed, and one of the is the finFET.

Fabrication of finFET in nanometer dimension needs precise control of the physical dimensions, such as fin-height (W), fin-width (t_{Si}) and gate length (L_G), because finFET performance controlled by its dimension. However, fabrication also involves process variations, one of them is gate misalignment that leads to fin-width lateral variation.



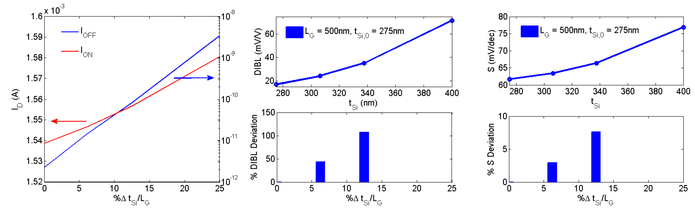
In general, gate misalignment introduces 2 effects on fin-width variations:
1. The increase in average fin-width
2. The introduction of a fin-width slope



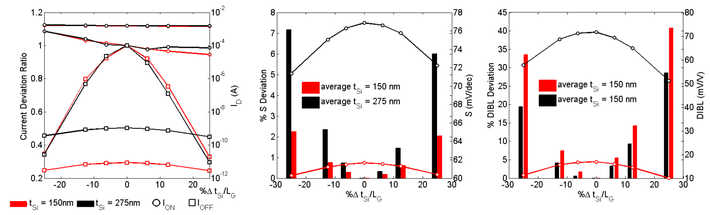
Measured as the percentage of variation with respect to gate length, the significance of both structural deviations on finFET performance are compared. The underlying effects in the subthreshold region is analysed based on the potential profile. Statistical study is also conducted to assess the performance variation in response to different degrees of gate misalignment.

Two Competing Effects of Gate Misalignment

1. Degradations due to Increasing Average Fin-Width



2. Improvements due to Tapering Fin-Width Structure



Subthreshold Peak Potential Shift due to Tapering Structure

Solving the Poisson's Equation while taking the dimensional variation into account gives us the potential profile expression of the transistor,

$$\frac{\mathrm{d}^2\phi(x,y)}{\mathrm{d}x^2} + \frac{\mathrm{d}^2\phi(x,y)}{\mathrm{d}y^2} = \frac{\mathrm{q}N_A}{\epsilon_{\mathrm{Si}}}$$

The potential in the transistor is

$$\phi(x,y) = u(x,y) + \psi(x,y)$$

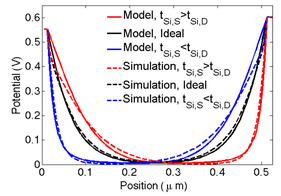
With $u(x,y)$ is the source and drain contribution and $\psi(x,y)$ is the gate contribution.

$$\psi(x,y) = \begin{cases} \Phi_G + \frac{qN_A t_{\mathrm{Si}}(x)}{2\epsilon_{ox}} y & ,0 \le y \le t_{ox} \\ \Phi_G + \frac{qN_A t_{\mathrm{Si}}(x) t_{ox}}{2\epsilon_{ox}} + \frac{qN_A t_{\mathrm{Si}}(x)}{2\epsilon_{\mathrm{Si}}}(y - t_{ox}) + \frac{qN_A}{2\epsilon_{\mathrm{Si}}}(y - t_{ox})^2 & ,t_{ox} \le y \le t_{ox} + t_{\mathrm{Si}}(x) \\ \Phi_G + \frac{qN_A t_{\mathrm{Si}}(x)}{2\epsilon_{ox}}(t_{\mathrm{Si}}(x) + 2t_{ox} - y) & ,t_{\mathrm{Si}}(x) + t_{ox} \le y \le t_{\mathrm{Si}}(x) + 2t_{ox} \end{cases}$$

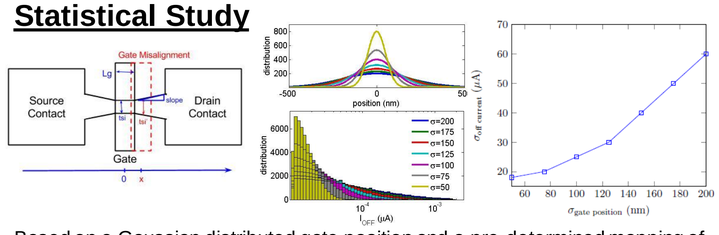
$$u(x,y) = \sum_n \sin\left(\frac{n\pi}{W_T} y\right) \frac{a_n \exp\left(\frac{n\pi}{W_T} x\right) + c_n \exp\left(\frac{n\pi}{W_T}(L-x)\right)}{2\sinh\left(\frac{n\pi}{W_T} L\right)}$$

The term $t_{\mathrm{Si}}(x) = \overline{t_{\mathrm{Si}}} - a(L - 2x)$ accounts for the thickness variation, which also appears in a_n, c_n and W_T.

As shown in the graph for long channel transistor lateral potential, the model predicts that potential is affected by the dimension variation, and accordingly influences other parameters



Sensitivity to Gate Misalignment Based on a Statistical Study



Based on a Gaussian distributed gate position and a pre-determined mapping of gate position to a modified fin-width and its tapering slope as shown in the figure above, it is shown that the distribution of off-current responds similarly to the underlying gate misalignment-distribution. This can also be seen from the positive relationship between the two standard deviations.

Conclusion

Two opposing effects of a laterally misaligned gate of a finFET are performance degradation from the overall increase in fin-width and better performance from the tapering structure. The former dominates (>2 times more significant), while the latter introduces a new physical phenomenon of maximum electrostatic potential shift. The amount of variation in performance parameters is also directly proportional to the underlying variation of lateral gate position.